# CPO Statement of Mentor Graphics

**Following the prerequisites of ProSTEP iViP's Code of PLM Openness (CPO) IT vendors shall determine and provide a list of their relevant products and the degree of fulfillment as a "CPO Statement" (cf. CPO Chapter 2.8).**

**This CPO Statement refers to:**

| | |
|---|---|
| **Product Name** | **Questa SIM** |
| **Product Version** | **Version 10** |
| | |
| **Contact** | **Ellie Burns**<br>**Ellie_burns@mentor.com** |

**This CPO Statement was created and published by Mentor Graphics in form of a self-assessment with regard to the CPO.**

**Publication Date of this CPO Statement: 17 June 2015**

## Content

# 1 Executive Summary

Questa SIM is an IEEE compliant HDL simulator that supports the use of VHDL, Verilog, SystemVerilog, and SystemC languages. Our support of these standards ensures that IEEE compliant designs will be compatible with the Questa SIM product.

| **Company Name:** | Mentor Graphics | **Contact Person:** | Ellie Burns |
|---|---|---|---|
| **Product Name:** | Questa | | |

| **CPO Term** | **Fulfilled (100%)** | **Comments because of deviations** |
|---|---|---|
| 2.1 Interoperability | ☒ | Comments: Customer written code, IP, and third party products may all be used together in Questa SIM if they are IEEE compliant. |
| 2.2 Infrastructure | ☒ | Comments: Support exists for multiple platforms and OS |
| 2.3 Extensibility | ☒ | Comments: Support exists for various versions of GCC that are tested for compatibility and are documented in the release notes. Customers are able to use various third party products for managing grid-based simulations, or other languages such as Perl. The User Interface supports modifications via the use of TCL/Tk |
| 2.4 Interfaces | ☒ | Comments: Programming interface support exists for PLI, VPI, and Mentor proprietary FLI. These are all C or C++ compatible interfaces. |
| 2.5 Standards | ☒ | Comments: VHDL 2008 Exceptions – see vhdl2008 Technote under help menu. VPI is partially implemented – see the Verilog_VPI Technote |
| 2.6 Architecture | ☒ | Comments: Questa SIM is one product in the Questa family. Data can be shared between these products as well as various third party products |
| 2.7 Partnership | ☒ | Comments: Questa SIM has a number of partnerships. Mentor has an OpenDoor program to create, build, and foster such relationships. |

| | |
|---|---|
| List of inherent supported neutral standards | API: ☒C/C++<br>IEEE: VHDL - 1076-2008, 1164-1993, 1076.2-1996,<br>IEEE: Verilog - 1364-2005,<br>IEEE: SystemVerilog - 1800-2012<br>IEEE: SDF – Std 1497-2001, IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process<br>VITAL 2000 – IEEE 1976.4-2000<br>SystemC – IEEE Std 1666-2011<br>Unified Power Format<br>(UPF 1.0) - February 22, 2007<br>(UPF 2.0) – IEEE Std 1801-2009<br>(UPF 2.1) – IEEE Std 1801-2013<br>PSL – IEEE 1850-2005 |

# 2 Details of Self-Assessment

The following chapters summarize the results of the CPO-related self-assessment of Mentor Graphics with regard to Questa SIM.

## 2.1 CPO Chapter 2.1: Interoperability

2.1.1 Designs and third party IP that conform to IEEE will be compatible with Questa SIM as well as other IEEE compliant products. This ensures that a design can be moved between IEEE compliant products from different vendors allowing a high level of design portability.

http://www.mentor.com/products/fv/questa-verification-platform

2.1.2 User Data can be accessed through a variety of methods. Data can be written from Questa SIM under program control, such as by PLI, or via Tcl commands as UCDB or VCD.

2.1.3 Interface access

a. VCD (Value Change Dump) IEEE 1364-2005, provides both export and import (Extended VCD)
b. Compatibility testing between versions ensures VCD with work from one version of Questa SIM to the next.
c. Simulation results saved as a Dataset can shared with other installations of Questa SIM at the same site or elsewhere.
d. Code Coverage results can be written as a report of saved as UCDB for later use.
e. Tcl stimulus files can be shared with other Questa SIM users
f. DPI is implemented as defined in IEEE std 1800-2005
g. PLI is implemented as defined in IEEE Std 1364-2001
h. VPI is partially implemented as defined in IEEE Std 1364-2005 and IEEE Std 1800-2005 – see the Verilog_VPI.note for more information

2.1.4 Questa SIM

An API (Application Programming Interface) and DPI (Direct Programming Interface) are available through the IEEE standards:

- IEEE 1364-2005 and 1364-1995 (Verilog)
- IEEE 1800-2012, 1800-2009 and 1800-2005 (SystemVerilog)

The standard for SystemVerilog specifies extensions for a higher level of abstraction for modeling and verification with the Verilog hardware description language (HDL). This standard includes design specification methods, embedded assertions language, testbench language including coverage and assertions application programming interface (API), and a direct programming interface (DPI).

## 2.2 CPO Chapter 2.2: Infrastructure

2.2.1 Questa SIM is available on Windows and Linux in the following configurations:

- Platform
  - EM64T
    - 32bit and 64bit versions on SUSE Linux Enterprise Server 10 and 11
    - 32bit and 64bit versions on Red Hat Enterprise Linux 5, 6, and 7
  - X86
    - 32bit and 64bit versions on Windows 7 and 8
    - 32bit and 64bit versions on Red Hat Enterprise Linux 5, 6, and 7
  - AMD64
    - 32bit and 64bit versions on SUSE Linux Enterprise Server 10 and 11
    - 32bit and 64bit versions on RED Hat Enterprise Linux 5, 6, and 7

2.2.2 A major release of Questa SIM is provided each year. Announcements of planned changes to platform/OS support are provided a year in advance with the annual major release of Questa SIM.

Product download and documentation is available to customers at the following location:

https://supportnet.mentor.com/login

## 2.3 CPO Chapter 2.5: Standards

2.3.1 Questa SIM is developed based on strict adherence to the following IEEE standards. Any product changes resulting from corrections or changes to these standards are documented in the product Release Notes.

- VHDL
  - IEEE Std 1076-2008, IEEE Standard VHDL Language Reference Manual

    Questa SIM supports the VHDL 2008 standard with a few exceptions. For detailed standard support information see the vhdl2008 technote available at <install_dir>/docs/technotes/vhdl2008.note, or from the GUI menu pull-down Help>Technotes>vhdl2008

    Potential migration issues and mixing use of VHDL 2008 with older VHDL code are addressed in the vhdl2008migration technote.

  - IEEE Std 1164-1993, Standard Multivalue Logic System for VHDL Model Interoperability
  - IEEE Std 1076.2-1996, Standard VHDL Mathematical Packages

    Any design developed with Questa SIM will be compatible with any other VHDL system that is compliant with the 1076 specifications.

- Verilog and SystemVerilog

- IEEE Std 1364-2005, IEEE Standard for Verilog Hardware Description Language
- IEEE Std 1800-2012, IEEE Standard for SystemVerilog – Unified Hardware Design, Specification, and Verification Language

Both PLI (Programming Language Interface) and VCD (Value Change Dump) are supported for Questa SIM users.

- SDF and VITAL
  - SDF – IEEE Std 1497-2001, IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process
  - VITAL 2000 – IEEE 1076.4-2000, IEEE Standard for VITAL ASIC Modeling Specification

- SystemC
  - IEEE Std 1666-2011, SystemC Language Reference Manual

- Unified Power Format (UPF)
  - (UPF 1.0) The Accellera Unified Power Format (UPF) Standard Version 1.0 – February 22, 2007
  - (UPF 2.0) IEEE Std 1801-2009 – Standard for Design and Verification of Low Power Integrated Circuits – March 27, 2009
  - (UPF 2.1) IEEE Std 1801-2013 – Standard for Design and Verification of Low Power Integrated Circuits – May 29, 2013

Questa SIM supports most of the UPF 1.0 and UPF 2.0 features. Support details are summarized in the Power Aware User's Manual.

- PSL
  - IEEE 1850-2005, IEEE Standard for Property Specific Language (PSL). For exceptions, see the Verification with Assertions and Cover Directives chapter.

.

## 2.4 CPO Chapter 2.6: Architecture

The Tcl GUI frontend of Questa SIM can be extensively modified for interactive use if so desired. Otherwise you can run the Questa SIM simulator in a batch mode or interactive mode. There is also an MC2 option that allows you modify the design to take advantage of the multi-core CPUs. Yes ☒ / No ☐

Otherwise there is no other direct modification available to the user. Any other interface or modification has to be accomplished through the use of the supported HDL languages, SystemC, or the Interfaces that are available through the various languages (PLI, DPI, VPI, or FLI).

## 2.5 CPO Chapter 2.7: Partnership

### 2.5.1 Data Generated by Users of Quest SIM

Data generated by Questa SIM users is and remains the intellectual property of the Questa SIM users. (CPO 2.7.4) Yes ☒ / No ☐

### 2.5.2 Partnership Models

Mentor Graphics has a partnership program available to customers and third party vendors. Yes ☒ / No ☐

http://www.mentor.com/company/partner_programs/opendoor/

### 2.5.3 Support of User and Innovation Groups

Mentor Graphics OpenDoor Partner index can be found at:

http://www.mentor.com/company/partner_programs/opendoor/partners_index/